WHAT IS CLAIMED IS:

1. A dynamic random access memory device comprising:

a bit line pair including a first bit line and a second bit line;

a first plurality of memory cells coupled to the first bit line;

a second plurality of memory cells coupled to the second bit line;

a sense amplifier coupled between the first bit line and the second bit line

a first characterization cell coupled between the first bit line and a first reference supply line, the first characterization cell including a first capacitor having a first capacitance value; and

a second characterization cell coupled between the first bit line and the first reference supply line, the second characterization cell including a second capacitor having a second capacitance value, the second value being different than the first capacitance value.

2. The device of claim 1 and further comprising:

a third characterization cell coupled between the second bit line and a second reference supply line, the third characterization cell including a third capacitor having a third capacitance value; and

a fourth characterization cell coupled between the second bit line and the second reference supply line, the fourth characterization cell including a fourth capacitor having a fourth capacitance value, the fourth capacitance value being different than the third capacitance value.

3. The device of claim 2 when the first capacitance value is substantially equal to the third capacitance value and when the second capacitance value is substantially equal to the fourth

capacitance value.

4. The device of claim 2 wherein:

the first characterization cell includes a transistor coupled between the first reference supply line and a storage node of the first capacitor, the transistor being controlled by a precharge signal;

the second characterization cell includes a transistor coupled between the first reference supply line and a storage node of the second capacitor, the transistor being controlled by the precharge signal;

the third characterization cell includes a transistor coupled between the second reference supply line and a storage node of the third capacitor, the transistor being controlled by the precharge signal; and

the fourth characterization cell includes a transistor coupled between the second reference supply line and a storage node of the fourth capacitor, the transistor being controlled by the precharge signal.

5. The device of claim 2 wherein:

the first characterization cell includes a first pass transistor coupled between a cell storage node and the first bit line;

the second characterization cell includes a second pass transistor coupled between a cell storage node and the first bit line, the second pass transistor being controlled independently of the first pass transistor;

the third characterization cell includes a third pass transistor coupled between a cell storage node and the second bit line, the third pass transistor being actuated at the same time as the first pass transistor; and

the fourth characterization cell includes a fourth pass transistor coupled between a cell storage node and the second bit line, the fourth pass transistor being actuated at the same time as the second pass transistor.

6. The device of claim 1 wherein the second capacitance value is an integer multiple of the first capacitance value.

7. The device of claim 1 wherein the first characterization cell includes a first pass transistor coupled between a cell storage node and the first bit line and the second characterization cell includes a second pass transistor coupled between a cell storage node and the second bit line, the first pass transistor being controlled independently of the second pass transistor.

8. A dynamic random access memory circuit capable of operating in either a test mode or a normal mode, the dynamic random access memory circuit comprising:

a first memory cell, a first characterization cell, and a second characterization cell coupled to a first bit line;

a second memory cell, a third characterization cell, and a fourth characterization cell coupled to a second bit line; and

a sense amplifier for sensing a voltage differential appearing between the first bit line and the second bit line and outputting a signal indicative of the sensed voltage differential;

wherein during the normal mode the first memory cell is selectively enabled to transfer a first memory charge onto the first bit line and the second memory cell is selectively enabled to transfer a second memory charge onto the second bit line, and the output signal provides a logic level relating to the transferred memory charge;

wherein during a first test mode the first characterization cell is selectively enabled to transfer a predetermined first reference charge onto the first bit line and the third characterization cell is simultaneously selectively enabled to transfer a predetermined second reference charge that is different from the first reference charge by an increment onto the second bit line, and the output signal provides information relating to a sensitivity of the sense amplifier; and

wherein during a second test mode the second characterization cell is selectively enabled to transfer a predetermined third reference charge onto the first bit line and the fourth characterization cell is simultaneously selectively enabled to transfer a predetermined fourth reference charge that is different from the third reference charge by an increment onto the second bit line, and the output signal provides information relating to a sensitivity of the sense amplifier.

9. The circuit of claim 8 wherein during the second test mode the first characterization cell and the third characterization cell are also selectively enabled.

10. The circuit of claim 8 wherein during the first test mode the increment is detected to determine the sensitivity of the sense amplifier by independently controlling the voltage differential appearing between the first bit line and the second bit line and by monitoring at least one output signal generated by the sense amplifier in response to sensing the voltage differential, wherein the voltage differential appearing between the first bit line and the second bit line is independently controlled during at time in which the first and second memory cells are not enabled.

11. A memory device comprising:

a plurality of bit line pairs, each bit line pair including an even bit line and an odd bit line;

a plurality of memory cells, each memory cell being coupled to one of the even or the odd bit lines such that each bit line has an equal number of memory cells coupled to it;

a plurality of sense amplifiers, each sense amplifier coupled to a corresponding one of the bit line pairs;

an even reference supply line;

an odd reference supply line;

for each even bit line, at least one characterization cell coupled between the even reference supply line and the particular even bit line;

for each odd bit line, at least one characterization cell coupled between the odd reference supply line and the particular odd bit line;

wherein, at least during a test mode, the even reference supply line is characterized by having a distributed resistance along the even reference supply line.

12. The device of claim 11 wherein the even reference supply line includes a first end and a second end, the first end coupled to a test node that receives a test voltage.

13. The device of claim 12 wherein, the second end of the even reference supply line is coupled to a second test node coupled to receive a second test voltage.

14. The device of claim 13 wherein the test voltage is different than the second test voltage.

15. The device of claim 14 wherein the test voltage is the same as the second test voltage.

16. The device of claim 11 wherein, at least during the test mode, the odd reference supply line is characterized by having a distributed resistance along the odd reference supply line.

17. The device of claim 11 and further comprising at least one switch coupled between the odd reference supply line and the even reference supply line.

18. The device of claim 17 wherein the at least one switch comprises a switch coupled between a first end of the odd reference supply line and a first end of the even reference supply line.

19. The device of claim 18 wherein the at least one switch further comprises a second switch coupled between a second end of the odd reference supply line and a second end of the even reference supply line.

20. The device of claim 17wherein the at least one switch comprises a plurality of switches coupled at select points between the odd reference voltage line and the even reference voltage line to allow creation of a different gradient between the reference voltage lines.

21. A method of testing a memory device that includes a plurality of bit line pairs, each pair including an even bit line coupled to an even reference supply line by a test cell and an odd bit line coupled to an odd reference supply line by a test cell, the memory device further including a plurality of sense amplifiers, each sense amplifier coupled to a respective one of the bit line pairs, the method comprising:

generating an even test voltage on the even reference supply line, the even test voltage being a function of physical location along the even reference supply line;

generating an odd test voltage on the odd reference supply line; the odd test voltage being a function of physical location and along the odd reference line; and

testing at least one of the sense amplifiers using at least one test cell coupled to the even reference supply line and at least one test cell coupled to the odd reference supply line.

22. The method of claim 21 wherein the even test voltage is constant along the even reference supply line.

23. The method of claim 22 wherein the odd test voltage is constant along the odd reference supply line.

24 The method of claim 22 wherein the odd test voltage is a linear function of physical location along the odd reference supply line.

25. The method of claim 24 wherein the odd test voltage has the same value as the even test voltage at a location along the odd reference voltage line.

26. The method of claim 25 wherein the location along the odd reference voltage line is one end of the odd reference voltage line.

27. The method of claim 21 wherein the even test voltage is a linear function of physical location along the even reference supply line and the odd test voltage is a linear function of physical location along the odd reference supply line.

28. The method of claim 27 wherein the even test voltage has the same value as the odd test voltage at a location adjacent to a particular one of the bit line pairs.

29. The method of claim 28 wherein the particular one of the bit line pairs comprises a bit line pair at one end of the reference supply lines.

30. The method of claim 21 wherein the method comprises applying different voltages to each column and using a single row access to provide test information.

31. A method of determining the sensitivity of a sense amplifier located within a dynamic random access memory circuit that includes first and second characterization cells and a first memory cell coupled to a first bit line, and a third and fourth characterization cells and a second memory cell coupled to a second bit line, the method comprising:

isolating the first and second memory cells from transferring a memory charge to the first and second bit lines respectively;

placing a first reference charge within the first characterization cell;

placing a second reference charge within the third characterization cell, the second reference charge being different from the first reference charge;

transferring the first reference charge from the first characterization cell to the first bit line;

transferring the second reference charge from the second characterization cell to the second bit line;

sensing a first voltage differential appearing between the first bit line and the second bit line;

placing a third reference charge within the second characterization cell;

placing a fourth reference charge within the fourth characterization cell, the fourth reference charge being different from the third reference charge;

transferring the third reference charge from the second characterization cell to the first bit line;

transferring the fourth reference charge from the fourth characterization cell to the second bit line;

sensing a second voltage differential appearing between the first bit line and the second bit line; and

obtaining information about the sensitivity of the sense amplifier from the first voltage differential and the second voltage differential.

32. The method of claim 31 and further comprising transferring charge from the first characterization cell to the first bit line when transferring the third reference charge and transferring charge from the third characterization cell to the second bit line when transferring the fourth reference charge.

33. The method of claim 31 and further comprising independently controlling a magnitude of the first reference charge and independently controlling a magnitude of the second reference charge.

34. The method of claim 33 wherein the step of independently controlling further includes:

coupling a first voltage source to a first bond pad coupled to the first characterization cell;

charging a capacitor within the first characterization cell to the first reference charge using the first voltage source;

coupling a second voltage source to a second bond pad coupled to the third characterization cell; and

charging a capacitor within the third characterization cell to the second reference charge using the second voltage source.